Teaching a Cross-Disciplinary Nanocomputing Systems Course

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Abstract- The end of photolithography as the driver for Moore's Law is predicted within few years and different emerging technologies (mostly nanotechnology) are expected to replace the current CMOS-based system integration paradigm. As nanotechnology is emerging, there is a strong need for well-educated engineers in nanocomputing systems design, and research and education efforts are also called to overcome numerous nano-based systems issues. This paper proposes an interdisciplinary course in nanocomputing systems by introducing two emerging technologies: Crossbar-based Nano-Architecture and Quantum-Dot Cellular Automata (QCA). The goals of the course are to introduce our students to the design trends of computing systems in the nanotechnology era, and make them highly competitive in future engineering jobs market. The course will be offered as undergraduate seniors/graduate course.

Keywords: Nanocomputing, nanotechnology, crossbar architecture, QCA, carbon nano tube, silicon nano-wire, design

INTRODUCTION

Recent advances in Photolithographic techniques have made possible the miniaturization of electronic circuits. According to Moore's Law, the number of transistors per unit area will continue to double approximately every two years. However, the applicability of Moore's law will cease to continue as the pitch sizes approach molecular dimensions. It therefore becomes necessary to explore devices and technologies that can match these trends of an increase in transistors per area [1]. Among the new nanoscale technologies, crossbar-based nanoscale architecture and quantum-dot cellular automata (QCA) have some outstanding advantages [1-5].

In crossbar-based nanoscale architecture, a two dimensional array (nanoarray) formed by the intersection of two orthogonal sets of parallel and uniformly-spaced nanometer-sized wires [2, 10], such as carbon nano tubes (CNTs) and silicon nanowires (SiNWs). Experiments have shown that such wires can be aligned to construct an array with nanometer-scale spacing using a form of directed self-assembly. It is to achieve ultra-high density which has never been achieved by photolithography (a density of 10^{11} crosspoints per $1cm^{2}$ has been achieved [5]). A 4 × 4 nanoscale crossbar with decoder structure is shown in Figure 1.

Semiconducting CNTs and SiNWs exhibit electronic properties similar to those of conventional lithographic-scale CMOS devices in terms of electron and hole mobilities. Chemical passivation of SiO_x shell surrounding single crystal SiNW cores has been shown to significantly enhance conductance-gate voltage behavior making these wires highly suitable to be used as Field Effect Transistors [2], and in turn as building blocks for digital circuits. The electronic applications of NWs are based on diode and FET-like properties of NW junctions or *"Crosspoints"* in 2-D arrays, called as *Nanofabrics* or *Crossbars.* Crosspoints can be grouped to form a memory or logic device. It was shown that electro-mechanical switching devices using suspended nanotubes.

The crosspoints at the junctions are programmed using this "Bistable" property that they exhibit. Their ON-state behavior is similar to that of a diode. When the two wires forming a junction are in close contact, the junction resistance is very small; when the wires are far away, their resistance increases by a great extent (~33MΩ in one state

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and ~10kΩ in the other) [2-5,10]. A crosspoint can be programmed ON or OFF by applying a voltage differential of ~3.6V. The Crosspoint takes part in the evaluation of Boolean expressions in the state in which they show diode-like properties.

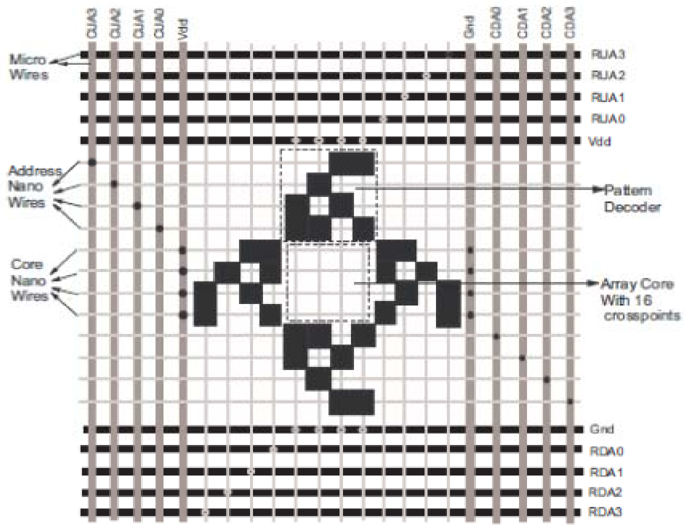
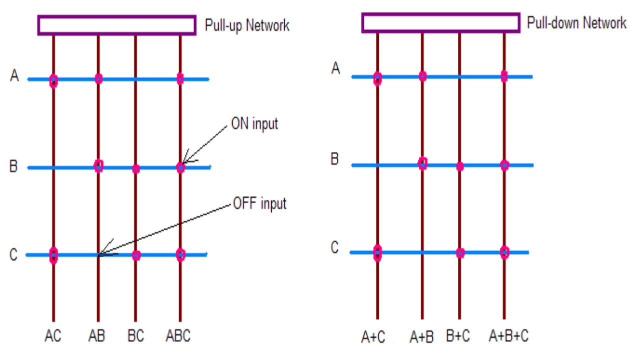


Figure1. A 4x4 nono-based crossbar architecture with imprinted pattern decoder

Figure 2 illustrates the setups for a Nano-crossbar as an AND array and OR array, respectively. The working is based on diode-like properties of crosspoints and the presence of a pull-up/pull-down network. The programmable crosspoints allow this network to implement logical sum/product terms on it. The inputs that take part in the evaluation of the sum/product terms are called ON inputs, and the ones that do not are called OFF inputs. Due to the presence of defects, these crosspoints may lose their programmability. Thus, if an ON input corresponds to a defective crosspoint, then it results in a faulty output. In addition, QCA can provide not only nanoscale system implementation, but also a new way of computation and information transformation. It is predicted that the density of



(a) **(b)**

Figure 2. (a) AND-array, (b) OR-array

QCA could exceed 10^{12} devices per $1cm^2$ and the operating speed could reach THz domain [6]. Compared with conventional CMOS-based digital logic, QCA hold its logic state by the position of electronics instead of voltage level [6, 12]. Also, the information transformation is realized by Coulomb interaction between adjacent QCA cells and the power dissipation is extremely low compared with CMOS technology.

Although there is a strong need for education and research in nanotechnology, both undergraduate and graduate-level courses of current science and engineering curricula usually do not properly include topics related to it. In this paper, we present a way to introduce nanotechnology in our undergraduate and graduate levels as a cross-disciplinary subject.

PROPOSED EDUCATIONAL MODULES

BACKGROUND

Nanotechnology is an interdisciplinary field. A course in nanocomputing systems in Electrical and Computer engineering curricula must allow students to synthesize engineering concepts from nano material properties, process design, and instrumentation in addition to the electronic circuit analysis, digital systems design, building computing blocks, and product design. It is essential that students learn to identify disadvantages of nanotechnology and how to deal with them at the same level of appreciating the advantages of the nanotechnology. The authors have adapted the Bloom's taxonomy shown in Figure 3 in developing the educational modules of the proposed course. Due to this lack of material specific to nanotechnology in the core engineering courses as well as the disparity in learning levels in concepts important to nanotechnology among the three departments, students who take a senior elective in nanotechnology are unable to effectively design and fabricate a nanotechnology-based device. Most times, the faculty member teaching this senior elective ends up teaching a course which only involves lower level thinking skills (knowledge or comprehension levels). In our proposed course, we hope to widen the student's knowledge in nanotechnology up to the higher order thinking skills, which is the creating (evaluation) in Figure 3. Our objective is to take the students up to the level that they can design and analyze a simple nanocomputing system.

Figure 3. Bloom's taxonomy

EDUCATIONAL MODULES

The proposed course will be offered to senior undergraduate and graduate students. Students are anticipated to have enough knowledge in digital systems design and/or VLSI design. The tentative educational modules to be developed consist of the followings:

1. Nano materials, characterization and fabrication modules: 4 weeks

Dr. Khan will be preparing the education modules for this section. The tentative materials are:

A. Nano materials and characterization: This module will introduce the fundamental concepts of nanotechnology and will provide a broad overview of this field. This module will include the following sections:

- Definitions and historical perspective
- What is different at the nano scale and why is it important to study this
- Overview of characterization tools
- Scanning and transmission electron micsroscope: theory, operation and applications
- Scanning tunneling microscope: theory, operation and applications
- Atomic force microscope: theory, operation and applications
- Relation to other nanotechnology modules

B. Nanofabrication: Nanofabrication is typically viewed from two perspectives: topdown and bottom-up. The top-down approach leverages many of the tools developed for other industries such as semiconductor manufacturing. These tools have allowed researchers to create billions of transistors on a silicon chip that is no larger than a postage stamp. The bottom-up approach leverages chemistry and biology to create devices one molecule at a time. Researchers have taken inspiration from living organisms to produce simple devices through self-assembly. One of the greatest challenges remaining it nanofabrication is to link the top-down and bottom-up approaches in a method that is robust and commercializable [11]. This module will include the following sections:

- Definitions and historical perspective
- Overview of top-down tools and techniques
- Examples of top-down nanofabrication: ULSI, planar photonic crystals, etc.
- Overview of bottom-up tools and techniques
- Examples of bottom-up nanofabrication: CNTs, nanowires, quantum dots, etc.
- Bridging the gap between the two approaches

2. Nanocomputing systems modules: 10 weeks

This is the core modules for the course. Dr. Al-Assadi will be developing relative modules based on his published research. Students will learn who to design simple nanocomputing system such as the n x n crossbar architectures and QCA based digital designs. In addition, they learn how to solve the critical issues of testing and reliability of such systems. The following education modules will be developed:

A. Nanoelectronics: Nano devices such as carbon nano tubes (CNT) and Silicon nano wires (SiNWs) will be introduced. The following topics will be covered:

(a) FET (Field Effect Transitor) devices: Lieber et al have shown electro-mechanical switching devices using suspended nanotubes [4]. The NT-NT junction is bistable with an energy barrier between the two states. Doped SiNWs and CNTs exhibit FET (Field Effect Transistor) behavior [2].
(b) Interconnect: Both CNT and SiNW can be used as interconnects along with microscale metallic wires.
(c) Memory devices: One of more crosspoints can be used as memory devices, as well. Structures and operation principles can be discussed.

B. 2-dimentional crossbar structures:

Multiple CNTs and/or SiNWs can be assembled to form a crossbar structure, so that crosspoints can be used as storage or logic devices. Design and assembly issues can be demonstrated. The following modules will be covered:

(a) Nano-Micro interface: Most of currently proposed crossbar-based architectures also include microscale devices and interconnects. Thus, nano-micro interfacing methods should be taught.
(b) Yield, Defect and fault tolerance: In nano-crossbar systems, various defects and faults that are fully different from the ones found in CMOS technology are expected. Thus, defect and fault-tolerant issues should be discussed and possible techniques should be taught. We will use the techniques developed by the first author in introducing a new type of redundancy to a large n x n 2-D crossbar architectures that aimed at maximizing the yield and reducing the re-configuration time complexity [7-10].
(c) Testing and Design automation: The built-in self test (BIST) technique developed by the first author will be utilized to test for large 2-D crossbar arrays. In this module, we will develop algorithmic techniques to utilize a comprehensive design for design for test and reliability [7-8].

C. Quantum-Dot Cellular Automata (QCA):

The following QCA topics will be covered:
(a) QCA cell structure: Multiple quantum dots can be used to form a QCA cell. Then, two or more electrons can be placed. QCA hold its logic state by the position of electrons.
(b) Cell-to-cell electrostatic interaction: The polarization of one cell will be directly affected by the polarization of its neighboring cells. This interaction is known to show non-linear cell-to-cell response. Both intra and inter-cell behaviors can be discussed.
(c) QCA devices: Multiple QCA cells can be placed strategically to form logic devices such as MV (Majority Voter) and INV (Inverter). Various QCA logic gate can be introduced.
(d) 4-phase clocking: Presently, all QCA circuit proposals require a clock not only to synchronize and control information flow but the clock actually provides the power to run the circuit. The concept of clocking for QCA, referred to as the four-phase clocking, has been introduced in [6,12]. The four-phase clocking scheme emulates classical shift register behavior since a binary digit of information can be stored in each cell’s latched polarization.

3. Course Assignments and Design Project:

Homework problems will be assigned that promotes critical thinking and increase interaction between students. In addition, it will help in enhancing and sustaining intellectual growth among students. Also, several course projects will be designed, or given the students the chance to develop their own design project. Algorithmic design automation projects will be designed to cover topics specified in B-2 education modules. The students will be encouraged to write a technical paper based on their projects. The best four paper will be selected to be presented in the annual University of South Alabama Research Council (USARC) organizes poster exhibition.

CONCLUSION

In this paper, we propose education modules for a new course in nanocomputing systems in the Electrical and Computer Engineering curricula at the University of South Alabama. The course will cover wide aspects in nanotechnology that will provide students with solid knowledge and background required for future engineering market. The education modules are designed to attract students to this promising discipline.

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BIOGRAPHICAL INFORMATION

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Waleed K. Al-Assadi received a Ph.D. in Electrical Engineering with an emphasis in Computer Engineering from Colorado State University in 1996. He has been with the Department of Electrical & Computer Engineering at the University of South Alabama as an Assistant Professor since August 2010. Prior to that he was with Missouri University of Science and Technology His research interests include VLSI systems design, embedded systems, computer architecture, and digital systems design.

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